NCP3102C

Wide Input Voltage Synchronous Buck Converter

The NCP3102C is a high efficiency, 10 A DC-DC buck converter designed to operate from a 5 V to 13.2 V supply. The device is capable of producing an output voltage as low as 0.8 V. The NCP3102C can continuously output 10 A through MOSFET switches driven by an internally set 275 kHz oscillator. The 40-pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP3102C also incorporates an externally compensated transconductance error amplifier and a capacitor programmable soft-start function. Protection features include programmable short circuit protection and under voltage lockout (UVLO). The NCP3102C is available in a 40-pin QFN package.

Features

- Input Voltage Range from 4.5 V to 13.2 V
- 275 kHz internal oscillator
- Greater than 90% max efficiency
- Boost pin operates to 30 V
- Voltage mode PWM control
- 0.8 V + 1 % Internal reference voltage
- Adjustable output voltage
- Capacitor programmable soft-start
- 85% Max duty cycle
- Input under voltage lockout
- Resistor programmable current limit
- This is a Pb-Free device

Applications

- Servers / Networking
- DSP & FPGA power supply
- DC-DC regulator modules

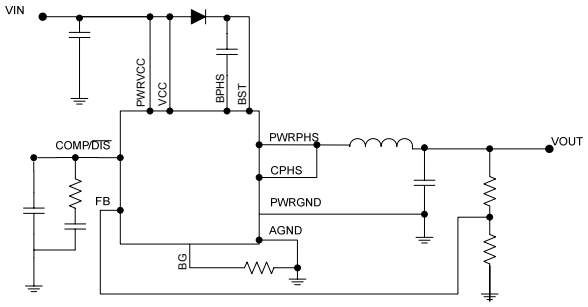
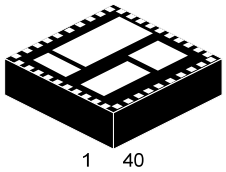


Figure 2. Typical Application Diagram

ON Semiconductor

http://onsemi.com

PACKAGE AND MARKING INFORMATION

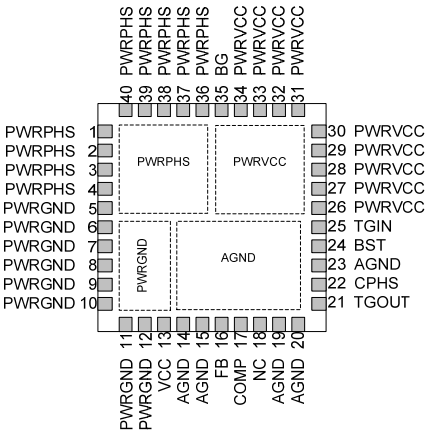


QFN40
CASE 485AK

NCP3102
AWLYYWW

A = Assembly Location
WL= Wafer Lot
YY= Year
WW = Work Week
G= Pb−Free Device

PIN CONNECTIONS



(Top View)

ORDERING INFORMATIOIN

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

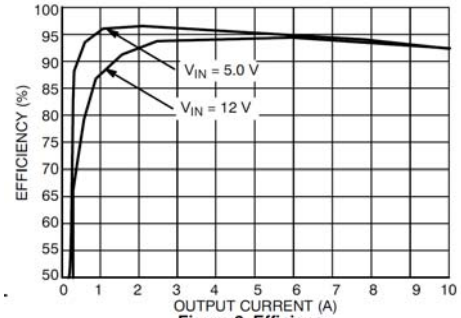


Figure 2. Efficiency

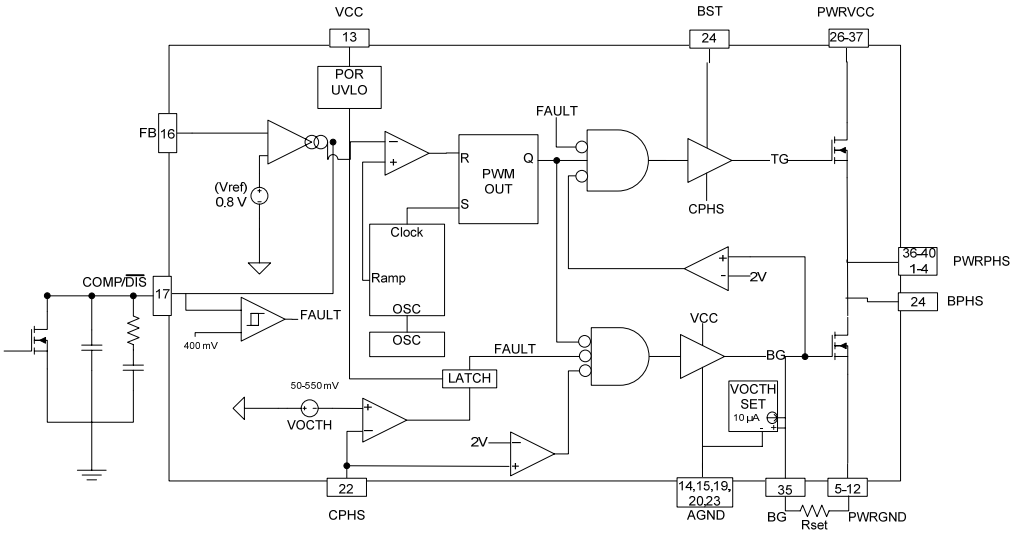


Figure 3. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1-4, 36-40	PWRPHS	Power phase node (PWRPHS). Drain of the low side power MOSFET.
5 -12	PWRGND	Power ground. High current return for the low-side power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors.
13	VCC	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 µF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
14,15,19, 20,23	AGND	IC ground reference. All control circuits are referenced to this pin.
16	FB	The inverting input pin to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage-control feedback loop. Connect this pin to the output resistor divider (if used) or directly to Vout.
17	COMP/DIS	Compensation or disable pin. The output of the error amplifier (EA) and the non-inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage-control feedback loop. The compensation capacitor also acts as a soft start capacitor. Pull the pin below 400mV to disable controller.
18	NC	Not Connected. These pins can be connected to AGND or not connected
21	TGOUT	Output high side MOSFET driver.
22	CPHS	The controller phase sensing for short circuit protection.
24	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (C_{BST}) between this pin and the BPHS pin.
25	BPHS	Drive signal to boost the input voltage for the high side driver. Should be conned to the boost capacitor and the boost diode
26-34	PWRVCC	Input supply pin for the high side MOSFET. Connect VCCPWR to the VCC pin.
35	BG	The current limit set pin. The current limit can be set be placing a 5 kΩ-30kΩ resistor to AGND which sets a 5 A and 30 A current limit accordingly

Table 2: MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Main Supply Voltage Input	V_{CC}	-0.3	15	V
Main Supply Voltage Input	PWRVCC	-0.3	30	V
Bootstrap Supply Voltage vs Ground	VBST	-0.3	35	V
Bootstrap Supply Voltage vs Ground (spikes < = 50 ns)	VBST spike	-5.0	40	V
Bootstrap Pin Voltage vs V_{PWRPHS}	VBST− PHS	-0.3	15	V
High Side Switch Max DC Current	I PHS	0	12	A
V_{PWRPHS} Pin Voltage	V_{PWRPHS}	-0.7	30	V
V_{PWRPHS} Pin Voltage (spikes < 50ns)	$V_{PWRPHSSP}$	-5	40	V
CPHASE Pin Voltage	V_{CPHS}	-0.7	30	V
CPHASE Pin Voltage (spikes < 50ns)	V_{CPHSTR}	-5	40	V
Current limit set and Bottom Gate	V_{BG}	-0.3	VCC < VSG < 15	V
Current limit set and Bottom Gate (spikes < 200ns)	V_{BGSP}	-2.0	VCC < VSGSP < 15	V
Top Gate vs Ground	V_{TG}	-0.3	30	V
Top Gate vs Phase	V_{TG}	-0.3	VCC < VTG < 15	V
Top Gate vs Phase (spikes < 200ns)	V_{TGSP}	-2.0	VCC < VTGSP < 15	V
FB Pin Voltage	VFB	-0.3	VCC < VFB < 5.5	V
COMP/DISABLE	VCOMP/DIS	-0.3	VCC < VCOMP/DIS < 5.5	V
Rating	**Symbol**	**Symbol**		**Unit**
Thermal Resistance, Junction−to−Ambient (Note2) (Note3)	$R_{\theta JA}$	35		°C /W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	55		°C /W
Storage Temperature Range	T_{stg}	-55 to 150		°C
Junction Operating Temperature	T_J	-40 to 150		°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free	RF	260 peak		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.

2. The value of θJA is measured with the device mounted on 1 in^2 FR−4 board with 1 oz. copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

3. The value of θJA is measured with the device mounted on minimum footprint, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

4. 60−180 seconds minimum above 237°C.

Table 3: ELECTRICAL CHARACTERISTICS (-40°C < T_J < 125°C; V_{IN} =12 V, BST− V_{SW} =12 V, BST = 12 V, V_{SW} = 24 V, for min/max values unless otherwise noted).

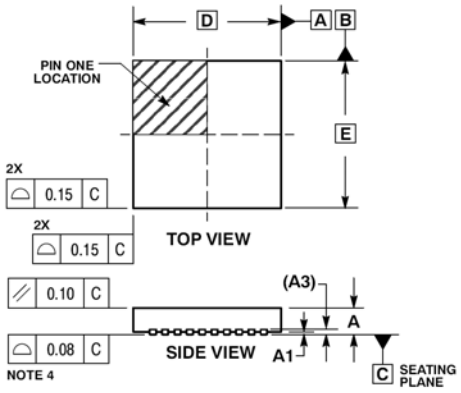
Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN} − GND	4.5		13.2	V
Boost Voltage Range	VBST − GND	4.5		26.5	V
Supply Current					
Quiescent Supply Current	VFB = 0.85V, No Switching, V_{IN} = 13.2V	3	-	5	mA
Quiescent Supply Current	VFB = 0.85V, No Switching, V_{IN} = 5.0V		3.2		mA
V_{CC} Supply Current	VFB = 0.75V, Switching, V_{IN} = 13.2V		26	32	mA
V_{CC} Supply Current	VFB = 0.75V, Switching, V_{IN} = 5V		11.1	13.1	mA
Boost Quiescent Current	VFB = 0.85V, No Switching, V_{IN} = 13.2V	0.1	-	1.0	mA
Shutdown Supply Current	VFB = 0V, No Switching, V_{IN} = 13.2V	-	4.0	-	mA
Under Voltage Lockout					
VIN UVLO Threshold	VIN Rising Edge	3.5	-	4.1	V
VIN UVLO Hysteresis	-	-	340	-	mV
Switching Regulator					
VFB Feedback Voltage, Control Loop in Regulation	0°C < TJ < 70°C, 4.5 V < VCC < 13.2 V −40°C < TJ < 125°C, 4.5 < VCC < 13.2 V	0.792 0.784	0.800 0.800	0.808 0.816	V
Oscillator Frequency	0°C < TJ < 70°C, 4.5 V < VCC < 13.2 V −40°C < TJ < 125°C, 4.5 < VCC < 13.2 V	250 223	275 275	300 337	kHz
Ramp−Amplitude Voltage		1	1.1	1.2	V
Minimum Duty Cycle		-	8.8	-	%
Maximum Duty Cycle		83	85	88	%
TG Falling to BG Rising Delay	VCC = 12 V, TG < 2.0 V, BG > 2.0 V		46	55	ns
BG Falling to TG Rising Delay	VCC = 12 V, BG < 2.0 V, TG > 2.0 V		41	49	ns
PWM Compensation					
Transconductance		3.2	-	3.6	mmho
Open Loop DC Gain	CO = 1 nF (Note 5)	55	70	-	DB
Output Source Current Output Sink Current	VFB < 0.8 V VFB > 0.8 V	88 80	139 130	193 175	µA
Input Bias Current		-	0.160	1.0	µA
Enable					
Enable Threshold (Falling)		0.37	0.4	.43	V
Soft-Start					
Delay to Soft−Start		5	-	14	ms
SS Source Current	V_{FB} < 0.8 V	6	10.5	15	µA
Switch Over Threshold	V_{FB} = 0.8 V	-	100	-	% of Vref
Over−Current Protection					
OCSET Current Source	Sourced from ISET pin, before SS	-	10	-	µA
OC Threshold	RBG = 5 kΩ		50		mV
OC Switch−Over Threshold	(Note 5)	-	700	-	mV
Fixed OC Threshold		-	96	-	mV
PWM Output Stage					
High-Side Switch On-Resistance	V_{IN} = 12V I_D= 1A		8		mΩ
Low-Side Switch On-Resistance	V_{IN} = 12V I_D= 1A		8		mΩ

Note:

5. Guaranteed by design

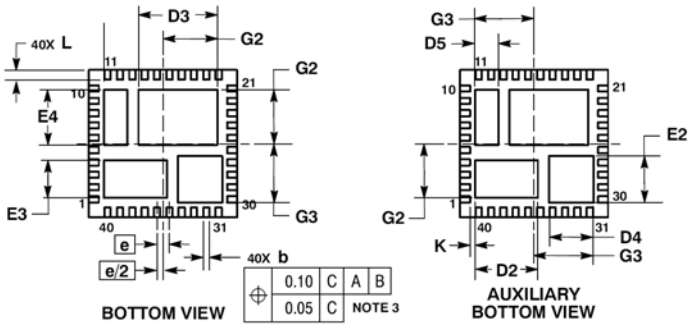
PACKAGE DIMENSIONS

QFN40 6x6, 0.5P
CASE 485AK–01
ISSUE A

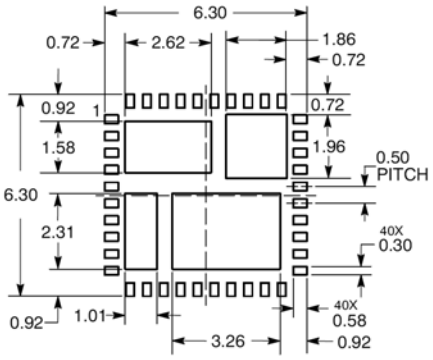


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.45	2.65
D3	3.10	3.30
D4	1.70	1.90
D5	0.85	1.05
E	6.00 BSC	
E2	1.80	2.00
E3	1.43	1.63
E4	2.15	2.35
e	0.50 BSC	
G2	2.10	2.30
G3	2.30	2.50
K	0.20	---
L	0.30	0.50



SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS